Amendments to the Specification:

Please amend the specification by inserting the following paragraph prior to the first existing paragraph in the specification:

- -This application is a divisional co-pending of U.S. Patent Application Serial No. 10/020,316, filed October 29, 2001, which is a divisional of U.S. Patent Application Serial No. 09/340,530, filed June 28, 1999, now U.S. Patent 6,617,681. - -

Please replace the second full paragraph on page 13, with the following amended paragraph:

- - Referring now to Fig. 9, a SiO_2 layer **214** is deposited to a thickness of approximately 5μ and disposed superjacent to silicon nitride layer **208**. A masking layer (not shown), typically comprising photoresist, is then formed and patterned superjacent to SiO_2 layer **214**. The pattern used is one which corresponds to trenches which are to be formed in oxide layer **214** and nitride layer **208** to facilitate a damascene copper metallization operation. Once the patterned masking layer is formed, exposed portions of oxide layer **214** are etched. This in turn exposes portions of nitride layer **208**. The photoresist masking layer may then be removed. The exposed portions of nitride layer **208** are then etched. A copper barrier layer and a copper seed layer are then deposited over the chip-side surface of the interposer including into the trench formed by the etching of the oxide layer **214** and nitride layer **208** described above. A copper layer ~~**215**~~ is electroplated over the copper seed layer. Copper layer ~~**215**~~ substantially fills the trench and covers the surface of the barrier layer deposited over oxide layer **214**. A planarization operation is then performed which polishes copper layer ~~**215**~~ back such that excess copper and the corresponding underlying portions of the barrier layer are removed from the surface of oxide layer **214**. This planarization/polish back operation is typically achieved by chemical mechanical polishing (CMP). Different slurry chemistries may be used for polishing the copper and the barrier layer in order to optimize the polishing operation. Subsequently, a silicon nitride layer **216** is deposited over copper layer ~~**215**~~ and oxide

layer **214** as shown in Fig. 9. Silicon nitride layer **216** is typically formed by a PECVD operation and formed to a thickness of approximately 0.1μ. - -